CLAIMS

1. A memory circuit comprising:

a plurality of memory cells, organized into columns and rows, that are accessed during memory access cycles, which include refresh cycles and read/write cycles, wherein the memory cells are substantially continuously refreshed using the refresh cycles;

a plurality of sense amplifiers, wherein each said sense amplifier is coupled to a corresponding one of the columns of the memory cells, and is used to read data stored in the memory cells of the corresponding column during read phases of the memory access cycles; and

a plurality of write amplifiers, wherein each said write amplifier is coupled to a corresponding one of the columns of the memory cells of the corresponding column, and is used to write data to the memory cells during write phases of the memory access cycles,

wherein the read phases of the refresh cycles substantially coincide with the write phases of the read/write cycles, and the write phases of the refresh cycles substantially coincide with the read phases of the read/write cycles.

2. The memory circuit of claim 1, further comprising a read/write address generator for generating read and write addresses.

3. The memory circuit of claim 2, further comprising a refresh address generator for generating refresh addresses used to refresh the memory cells.

4. The memory circuit of claim 3, further comprising a collision avoidance mechanism, which prevents an attempt to perform both refresh and read/write operations concurrently on identical said memory cells.

5. The memory circuit of claim 4, wherein the collision avoidance mechanism compares the refresh addresses with the read/write addresses to determine whether the attempt is made to perform both the refresh and read/write operations concurrently on the identical said memory cells.

6. The memory circuit of claim 5, wherein at least one of the refresh addresses is updated to prevent the attempt to perform both the refresh and read/write operations concurrently on the identical said memory cells.

7. The memory circuit of claim 6, wherein the at least one of the refresh addresses is updated by being changed by at least one.

8. A method of refreshing memory cells organized into columns and rows, the memory cells being accessed during memory access cycles, which include refresh cycles and read/write cycles, the method comprising:

reading data stored in the memory cells during read phases of the memory access cycles; and

writing data to the memory cells during write phases of the memory access cycles,

wherein the memory cells are substantially continuously refreshed, and

wherein the read phases of the refresh cycles

substantially coincide with the write phases of the read/write cycles, and the write phases of the refresh cycles substantially coincide with the read phases of the read/write cycles.

9. The method of claim 8, further comprising generating read and write addresses.

10. The method of claim 9, further comprising generating refresh addresses used to refresh the memory cells.

11. The method of claim 10, further comprising preventing an attempt to perform both refresh and read/write operations concurrently on identical said memory cells.

12. The method of claim 11, wherein preventing comprises comparing the refresh addresses with the read/write addresses to determine whether the attempt is made to perform both the refresh and read/write operations concurrently on the identical said memory cells.

13. The method of claim 12, wherein preventing further comprises updating at least one of the refresh addresses to prevent the attempt to perform both the refresh and read/write operations concurrently on the identical said memory cells.

14. The method of claim 13, wherein updating comprises changing the at least one of the refresh addresses by at least one.

15. A system-on-chip (SOC) device comprising:

data processing circuitry for processing input data to

generate output data;

an I/O port for receiving the input data and for outputting the output data; and

a memory block comprising:

a plurality of memory cells, organized into columns and rows, that are accessed during memory access cycles, which include refresh cycles and read/write cycles, wherein the memory cells are substantially continuously refreshed using the refresh cycles;

a plurality of sense amplifiers, wherein each said sense amplifier is coupled to a corresponding one of the columns of the memory cells, and is used to read data stored in the memory cells of the corresponding column during read phases of the memory access cycles, wherein the data processing circuitry processes the input data based on the data stored in the memory cells to generate the output data; and

a plurality of write amplifiers, wherein each said write amplifier is coupled to a corresponding one of the columns of the memory cells of the corresponding column, and is used to write data to the memory cells during write phases of the memory access cycles,

wherein the read phases of the refresh cycles substantially coincide with the write phases of the read/write cycles, and the write phases of the refresh cycles substantially coincide with the read phases of the read/write cycles.

16. The SOC device of claim 15, wherein the memory block further comprises a read/write address generator for generating read and write addresses.

17. The SOC device of claim 16, wherein the memory block

further comprises a refresh address generator for generating refresh addresses used to refresh the memory cells.

18. The SOC device of claim 17, wherein the memory block further comprises a collision avoidance mechanism, which prevents an attempt to perform both refresh and read/write operations concurrently on identical said memory cells.

19. The SOC device of claim 18, wherein the collision avoidance mechanism compares the refresh addresses with the read/write addresses to determine whether the attempt is made to perform both the refresh and read/write operations concurrently on the identical said memory cells.

20. The SOC device of claim 19, wherein at least one of the refresh addresses is updated to prevent the attempt to perform both the refresh and read/write operations concurrently on the identical said memory cells.

21. The SOC device of claim 20, wherein the at least one of the refresh addresses is updated by being changed by at least one.